



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
08/660,016	06/06/96	PIPPIN	J 042390.P1674

B3M1/0109
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BLVD SEVENTH FLOOR
LOS ANGELES CA 90025

EXAMINER	
SIEK, V	
ART UNIT	PAPER NUMBER
2304	12

DATE MAILED: 01/09/97

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

OFFICE ACTION SUMMARY

- ☒ Responsive to communication(s) filed on 6-6-96
- ☐ This action is FINAL.
- ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

- ☒ Claim(s) 1-19, 37-39 is/are pending in the application.
- Of the above, claim(s) _____ is/are withdrawn from consideration.
- ☐ Claim(s) _____ is/are allowed.
- ☒ Claim(s) 1-19, 37-39 is/are rejected.
- ☐ Claim(s) _____ is/are objected to.
- ☐ Claims _____ are subject to restriction or election requirement.

Application Papers

- ☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
- ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- ☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.
- ☐ The specification is objected to by the Examiner.
- ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- ☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been
- ☐ received.
- ☐ received in Application No. (Series Code/Serial Number) _____
- ☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

- ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

- ☒ Notice of Reference Cited, PTO-892
- ☒ Information Disclosure Statement(s), PTO-1449, Paper No(s) _____
- ☒ Interview Summary, PTO-413
- ☒ Notice of Draftsperson's Patent Drawing Review, PTO-948
- ☒ Notice of Informal Patent Application, PTO-152

→SEE OFFICE ACTION ON THE FOLLOWING PAGES→

Art Unit: 2304

DETAILED ACTION

1. This office action responds to the applicant's remark filed on 6/6/96. Claims 1-19 remain for examination. Claims 37-39 have been newly added (see paragraph 7).
2. Applicant's arguments filed on 6/6/96 have been fully considered but they are not deemed to be persuasive.
3. The disclosure is objected to because of the following informalities: on page 23, reference "programmable thermal sensor 100" is not in Fig. 7. Appropriate correction is required.
4. The numbering of claims is not accordance with 37 C.F.R. § 1.126. The original numbering of the claims must be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When claims are added, except when presented in accordance with 37 C.F.R. § 1.121(b), they must be renumbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 20-22 have been renumbered 37-39, respectively.

Art Unit: 2304

5. Claims 1-3, 8-10 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Giordano et al. (hereafter Giordano) U.S. Patent 5,359,236 in view of Nelson U.S. Patent 4,789,819 in further view of Kenny et al. U.S. Patent 5,287,292.

As to claims 1-3, 8-10 and 15, Giordano discloses an integrated circuit thermal sensor. As shown in Fig. 4, the well known integrated thermal sensor included precise CMOS bandgap voltage references which use the difference of MOS source-gate voltage to perform efficient curvature compensation have been designed and fabricated. Fig. 1A shows a portion of a bandgap voltage KV_{bg} being applied between the base and emitter of bipolar transistor Q1, also referred to as the controlled device. Generally, the bandgap voltage, KV_{bg} , applied to the base of Q1 is held at a relatively fixed value as a function of temperature, as shown in Fig. 1B. Temperature sensing is achieved by relying on the well known principle that the base-to-emitter voltage (V_{be}) of a bipolar transistor decreases at a predetermined rate (col 1, lines 26-38). Accordingly, Giordano discloses circuits embodying the invention include a means for generating a turn-on signal which increases with increasing temperature. This turn-on signal is applied to the control device whose turn-on threshold decreases with temperature. Giordano also discloses that the integrated thermal sensor includes a current source to generate the turn-on (or control) voltage (signal) which is increased

Art Unit: 2304

linearly as a function of increasing temperature (col 3, lines 2-5, col 5 and Figs. 2 & 4). Thus, this control voltage V14 is scaling to proportionally and linearly with increasing temperature. Additionally to the scaling of the sensing voltage of Giordano, Nelson discloses a voltage reference circuit including a well known Brokaw Cell bandgap reference circuit with breakpoint compensation to adjust the temperature coefficient of the reference voltage as a function of temperature. It is noted that in the design of an analog integrated circuit, it is necessary to establish a voltage or current reference which is substantially independent of variations in temperature. Therefore, a bandgap voltage reference circuit is often utilized to provide such a reference voltage or current. Nelson also discloses a scaling factor so as to obtain an output voltage with normally zero temperature dependence (col 1). Regarding to varying threshold voltage detection, Kenny discloses an integrated circuit to detect programmable threshold in order to sense the temperature of a CMOS integrated circuit. When the programmable threshold value is detected (predetermined temperatures), the CPU speed is decreased or increased accordingly (see summary). Therefore, with the motivation of detecting a programmable threshold according to temperature variation as taught by Kenny, one of ordinary skill in the art at the time the invention was made would have found it obvious to

Art Unit: 2304

combine the teachings of Giordano, Nelson and Kenny because this would save the cost of a cooling fan or heat sink since it is virtually free when implementing on an existing circuit as suggested by Kenny (col 5, lines 11-13) and then improve the thermal sensor performance.

6. Claims 4-7, 11-14 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Giordano et al. (hereafter Giordano) U.S. Patent 5,359,236 in view of Nelson U.S. Patent 4,789,819 in further view of Kenny et al. U.S. Patent 5,287,292 and Heck et al. (hereafter Heck) U.S. Patent 5,077,491. Giordano, Nelson and Kenny disclose the claimed invention except for step of scaling sensing voltage and comparison means. Giordano and Nelson suggest scaling sensing voltage using resistive elements R1 and R2 (col 5 of Giordano). It is noted that the CMOS bandgap voltage reference is well known in the art at the time the invention was made. Therefore, it would have been obvious matter of design choice to use MOSFET transistors coupled with resistive elements to provide a voltage scaling. Regarding to comparison means, Heck discloses a comparator circuit having a zero temperature coefficient with hysteresis. In general, a well known comparator circuit compares an input signal against a predetermined threshold value and switches between output states depending on whether the input signal is

Art Unit: 2304

above or below the trip threshold (also see summary). The teachings of Heck would motivate one of ordinary skill in the art at the time the invention was to incorporate a comparison means into the integrated thermal sensor of Giordano in order to generate a control signal or output signal because this would improve the performance of integrated thermal sensor.

7. Regarding to claims 37-39, the examiner understand that the Applicant tries to set up for the interference. Thus, the examiner respectfully submit that the interference's claims will be deferred to a later date.

Response to the applicant's remarks

Responding to the applicant's remark on page 4, that the teachings temperature detecting circuit of Cacciatore is external to the microprocessor, the examiner respectfully submit that Kenny clearly teaches the features within the microprocessor (see paragraph 5). Regarding to the integrated thermal sensor of Giordano is not programmable, and Nelson temperature independent output voltage is not programmable, the examiner respectfully disagree. Additionally, the teachings of Kenny clearly shows these features (see paragraph 5). Regarding to the feature of detecting the threshold temperature and programmable inputs, Kenny clearly teaches these features (see paragraph 5).

Serial Number: 08/660,016

-7-

Art Unit: 2304

8. The following references are cited by the examiner as of general interest.

a. Ristic et al., U.S. Patent 5,291,607 is cited to show a microprocessor having an integrated sensor (summary).

b. Salem, U.S. Patent 4,488,824 is cited to show a bandgap voltage reference and temperature sensor (summary).

c. Chin et al. "A New Type of Curvature-Compensated CMOS Bandgap Voltage References," IEEE, 1991, pp. 398-402.

d. Ferro et al. "A Floating CMOS Bandgap Voltage Reference for Differential Applications," IEEE, 1989, pp. 690-697.

e. Salminen et al. "The Higher Order Temperature Compensation of Bandgap Voltage References," IEEE, 1992, PP. 1388-1391.

Serial Number: 08/660,016

-8-

Art Unit: 2304

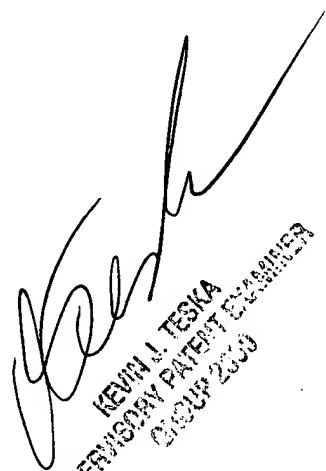
9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (703) 305-4958.

Any inquiry of general nature or relating to the status of this application should be directed to the group receptionist whose telephone number is (703) 305-9600.

VS

Art Unit 2304

December 31, 1996


KEVIN J. TESKA
SUPERVISORY PATENT EXAMINER
GROUP 2304